KLS Gogte Institute of Technology

Department of Information Science & Engineering

**Internal Assessment- III**

Subject: Logic Design Code: 15CS32

Semester: III Max. Marks: 25

Date: 11-11-2016 Duration: 1 Hour

**Note: Answer all 5 questions for 25 Marks.**

1. Analyse the circuit given below and find the output Y. [L4, CLO3, PO1]

2. Differentiate serial and parallel counters. Design a mod 8 ripple counter. [L4, L5, CLO3, PO1]

3. Define lock in condition. Design a synchronous mod 5 down counter [L1, L5, CLO3, PO1]

4. For a 5 bit ladder if the input levels are 0=0v and 1=+10v, calculate the following

1. Output voltages caused by each bit
2. Full scale output voltage
3. Output voltage for the input 11011 [L3, CLO3, PO1]

5. Develop the data flow verilog code for a (i) 2to1 mux (ii) D flip flops [L3, CLO3, PO1]

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Staff In charge Stream Leader

Prof. S.B.Deshpande Prof. P.S.Upparmani

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